IN THE CLAIMS:

1. (original) A method for fabricating a flash memory device comprising:

fabricating a gate structure comprising a tunnel oxide layer, a floating gate layer, an oxide layer, and a control gate layer on a semiconductor substrate, wherein said fabricating comprises an etch process, and wherein said etch process results damage to said tunnel oxide layer; ~~and~~

creating a first impurity concentration in said semiconductor substrate prior to said repairing;

creating a second impurity concentration in said semiconductor substrate prior to said repairing; and

repairing damage resulting from said etch process to said tunnel oxide layer prior to creating said first impurity concentration and creating said second impurity concentration, wherein said repairing said tunnel oxide layer is accomplished using a rapid thermal oxidation (RTO) process[[.]] , and wherein repairing said tunnel oxide layer prior to creating said first and second impurity concentrations prevents a dopant diffusion from said first and second concentration into a channel region due to said repairing.

2. (canceled)

3. (original) The method as recited in Claim 2, wherein said fabricating comprises fabricating a gate structure that is less than 0.21 microns (0.21μ) in length.

4. (original) The method as recited in Claim 1, wherein said repairing comprises:

creating additional oxide material in a damaged region of said oxide layer.

5. (original) The method as recited in Claim 1, wherein said rapid thermal oxidation process comprises exposing said semiconductor structure to a temperature of 1000°C for a period of time not longer than 20 seconds.

6. (original) The method as recited in Claim 1, wherein said rapid thermal oxidation process comprises selecting a plurality of process parameters wherein a portion of said tunnel oxide layer retains a uniform profile after said rapid thermal process is performed.

7. (previously presented) A method for fabricating a memory device comprising:

fabricating a gate structure upon a semiconductor substrate, wherein said fabricating comprises an etch process, wherein said gate structure comprises an tunnel oxide layer, and wherein said etch process results in damage to said oxide layer;

depositing a dopant in a first region of said semiconductor substrate and in a second region of said semiconductor substrate; and

performing a rapid thermal oxidation (RTO) process upon said semiconductor substrate prior to said depositing said dopant in said first region and said second region of said semiconductor substrate, wherein additional oxide material is created in

a damaged region of ~~an~~ said tunnel oxide layer of said gate structure[[.]] , and wherein said performing said RTO process prior to said depositing said dopant into said first and second regions prevents diffusion of said dopant into a channel region.

8. (original) The method as recited in Claim7, wherein said memory device comprises a flash memory device and comprising fabricating a floating gate memory structure upon said semiconductor substrate.

9. (original) The method as recited in Claim 8, wherein said fabricating comprises fabricating a floating gate structure that is less than 0.21 microns (0.21μ) in length.

10. (canceled)

11. (original) The method as recited in Claim 7, wherein said rapid thermal oxidation process comprises selecting a plurality of process parameters wherein a portion of said tunnel oxide layer retains a uniform profile after said rapid thermal process is performed.

12. (original) The method as recited in claim 11, wherein said rapid thermal oxidation process comprises exposing said semiconductor structure to a temperature of 1000°C for a period of time not longer than 20 seconds.

13. (previously presented)A method for fabricating a memory device comprising:

depositing a plurality of layers upon a semiconductor substrate, wherein said plurality of layers comprises a tunnel oxide layer;

patterning said plurality of layers to create a stack gate, wherein said patterning comprises an etch process, and wherein said etch process produces a damaged region of said tunnel oxide layer; ~~and~~

creating a source region wherein a first impurity concentration is deposited in said semiconductor substrate;

creating a drain region wherein a second impurity concentration is deposited in said semiconductor substrate; and

performing a rapid thermal oxidation (RTO) upon said stack gate prior to said creating said source region and said creating said drain region, wherein additional oxide material is created in ~~a~~ said damaged region of ~~an~~ said tunnel oxide layer of said stack gate[[.]] , wherein said performing said RTO prior to said creating said source and drain regions prevents a dopant diffusion into from said source and said drain regions into a channel region.

14. (canceled)

15. (original) The method as recited in Claim 14, wherein said patterning comprises creating a stack gate upon said semiconductor substrate is less than 0.21 microns (0.21μ) in length.

16. (canceled)

17. (original) The method as recited in Claim 16, wherein said rapid thermal oxidation process comprises selecting a plurality of process parameters wherein a portion of said tunnel oxide layer retains a uniform profile after said rapid thermal process is performed.

18. (original) The method as recited in Claim 17, wherein said rapid thermal oxidation process comprises exposing said semiconductor structure to a temperature of 1000°C for a period of time not longer than 20 seconds.